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<u>L32</u>	L26 and 19	39	<u>L32</u>
<u>L31</u>	L26 and 18	0	<u>L31</u>
<u>L30</u>	L26 and 17	5	<u>L30</u>
<u>L29</u>	L26 and 16	5	<u>L29</u>
<u>L28</u>	L26 and 15	15	<u>L28</u>
<u>L27</u>	L26 and 14	46	<u>L27</u>
<u>L26</u>	116 and instruction\$1 near6 decod\$4	198	<u>L26</u>
DB=PGPB,USPT; PLUR=YES; OP=OR			
<u>L25</u>	L24 and 116	110	<u>L25</u>
<u>L24</u>	(710/22,23)[CCLS]	1454	<u>L24</u>

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<u>L23</u>	L17 and I9	128	<u>L23</u>
<u>L22</u>	L17 and I8	2	<u>L22</u>
<u>L21</u>	L17 and I7	50	<u>L21</u>
<u>L20</u>	L17 and I6	50	<u>L20</u>
<u>L19</u>	L17 and I5	15	<u>L19</u>
<u>L18</u>	L17 and I4	54	<u>L18</u>
<u>L17</u>	L16 and (integrated or chip or semiconductor or monolithic) (gp or general near1 purpose near1 register\$1) near55 (dma or direct near1	808	<u>L17</u>
<u>L16</u>	memory near1 access\$3) and (reconfigur\$6 or configur\$6 or extension\$3 or extend\$5)	1355	<u>L16</u>
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>			
<u>L15</u>	I3 and I9	126	<u>L15</u>
<u>L14</u>	I3 and I8	2	<u>L14</u>
<u>L13</u>	I3 and I7	220	<u>L13</u>
<u>L12</u>	I3 and I6	220	<u>L12</u>
<u>L11</u>	I3 and I5	254	<u>L11</u>
<u>L10</u>	I3 and I4	516	<u>L10</u>
<u>L9</u>	(710/22-74)[CCLS]	11861	<u>L9</u>
<u>L8</u>	(711/112)[CCLS]	1963	<u>L8</u>
<u>L7</u>	(711/112-173)[CCLS]	25652	<u>L7</u>
<u>L6</u>	(711/112-173)![CCLS]	25652	<u>L6</u>
<u>L5</u>	(712/208-229)[CCLS]	6489	<u>L5</u>
<u>L4</u>	(712/2-300)[CCLS]	13389	<u>L4</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L3</u>	L2 and instruction\$1 near6 decod\$4	1882	<u>L3</u>
<u>L2</u>	L1 and (integrated or chip or semiconductor or monolithic). (gp or general near1 purpose near1 register\$1) and (dma or direct near1	14691	<u>L2</u>
<u>L1</u>	memory near1 access\$3) and (reconfigur\$6 or configur\$6 or extension\$3 or extend\$5)	22343	<u>L1</u>

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IEEE JNL IEEE Journal or Magazine

IET JNL IET Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IET CNF IET Conference Proceeding

IEEE STD IEEE Standard

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- ☐ 4. **An ASIC RISC-based I/O processor for computer applications**
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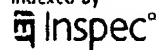
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